these amendments are not relied upon, however, to traverse the claim rejections. No new matter has been added.

Objections to Drawings

Paragraph 1 of the Office Action objects to the drawings under 37 CFR 1.83(a). In particular, the Office Action states that they fail to show: the mixer 72 (line 9, page 10), the inverter 174 (line 22, page 12); the reference voltage Vref (line 30, page 13), the reference voltages V2, V4, V6, V8 are connected to ground (line 30, page 13), the switches 148, 149 and 150 (line 23, page 20), the non overlapping four phase clock (line 16, page 27), the output of the input op amp (line 23, page 27); and the latch stage 804 (line 25, page 33) as described in the specification. According to the Action, any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing, citing MPEP § 608.02(d), and a correction is required.

In regard to the mixer, the specification has been amended to correct an error by replacing "mixer 72" with "mixer 74". This amendment brings the specification into conformance with the drawings (see FIG. 1).

Regarding the inverter, FIG. 5 has been amended to correct a reference designator. This amendment brings the drawings into conformance with the specification (see page 12, line 22).

In regard to the reference voltage V_{ref} and voltages V2, V4, V6, V8, Applicants point out that the specification, page 13, lines 30-31, states that "[i]n one embodiment, the reference voltages V1, V3, V5 and V7 are connected to a reference voltage V_{ref}, and reference voltages V2, V4, V6, V8 are connected to ground." This statement is clear to one of ordinary skill in the art. There is no need to show such an embodiment in the drawings. 37 CFR § 1.83(a) requires only that <u>claimed</u> elements be illustrated. There is no corresponding claim unsupported by a figure. FIG. 5 already shows V1, V3, V5, V7, V2, V4, V6, V8, and ground.

Regarding switches 148, 149 and 150 (line 23, page 20), the specification has been amended at page 20, line 23, to correct an error by replacing "a switch 148, a switch 149, and a switch 150" with "a switch S48, a switch S49, and a switch S50". This amendment brings the specification into conformance with the drawings (see FIG. 15) and the remainder of the specification (see page 20, lines 24-30). The specification has also been amended at page 20, line 22 to replace "FIGS. 9, 10A-10C" with "FIGS. 13, 14A-14C". This amendment brings the

specification into conformance with the drawings (see FIGS. 13, 14A-14C and 15) and the remainder of the specification (e.g., page 20, lines 24-30).

Regarding the non overlapping four-phase clock, the specification is clear to one of ordinary skill in the art. For example, FIG. 27 already includes references to phases of a non-overlapping four-phase clock (e.g., P1, P2, P3, P4). Moreover, FIG. 9 shows one embodiment of a non-overlapping four-phase clock. Consequently, the objection should be withdrawn.

Regarding the output of the input op amp, the specification is clear to one of ordinary skill in the art. For example, FIG. 27 shows two op amps in the switched capacitor filter 90. One of these op amps can clearly be viewed as an "input op amp". Moreover, the specification, at page 27, line 32, explicitly refers to "the input op amp of the SC filter stage 90." Consequently, the objection should be withdrawn.

In regard to the latch stage, FIG. 35 has been amended, pursuant to a drawing amendment enclosed herewith, to add a reference designator ("804") pointing to the latch stage. This amendment brings the drawings into conformance with the specification (see page 33, line 25).

Paragraph 2 of the Office Action objects to the drawings under 37 CFR 1.83(a). The Office Action states that the drawings must show every feature of the invention specified in the claims. Therefore, the features as recited in claims 5 and 13 must be shown or the feature(s) canceled from the claim(s).

Original claims 5, 13 recited "wherein there is a one to one relationship between a number of capacitors and a number of bits." Examples of this feature are already shown in the drawings, for example FIG. 5 (4 capacitors, 4 input bits) and FIG. 13 (4 capacitors, 4 input bits). Nonetheless, as stated above, claims 5, 13 have been amended to more particular point out and distinctly claim the inventions recited by these claims.

Claim Rejections Under 35 U.S.C. 112

Paragraph 4 of the Office Action rejects claim 1-65 under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

In particular, the Office Action states that claims 1-65 are not clearly understood because of the following reasons: the mixer circuit in Fig. 2 is not described; the QDAC1 to QDACN and the charge sharing network in Fig. 4 are not described; the elements 176 and P1 + P2 in Fig. 5 is

not described; Fig. 6 is not described; all equations in Figs. 7A-C, 8A-D and 12A-C, 14A-C, 19A-C, 33A-C and 34A-C are not clearly understood since the Vref and Q(C1), Q(C2), Q(C3) and Q(C4) are not described; the master clock and signal P4 in Fig. 9 are not described; the switch connected between element 164 and S19 in Fig. 10 is not described; the switching ON/OFF operation of all the switches in each of Figs. 11A-D, 15, 16A-E, 17-18, 19A-C, 20-22, 25, 27 and 30 is not understood since no switching control signal is shown and described; the connection of each of elements 202, 204, 206, 208 S49 and S50 in Fig. 15 is not completely described; the connection of each of elements S43 and S48 in Fig. 16A-E is not completely described; it is not clear how terminals 312 and 314 in Figs. 16B-E are interconnected with each other; elements NC, NAND gates inverters, switches, capacitors and terminals in Figs. 17, 21-22, 25 are not described as well as numbered; the four arrows on the right side of scrambler 400 in Fig. 24 are not described; the NAND gates and inverters in Fig. 26 are not described as well as numbered; all capacitors in Fig. 27 are not described as well as numbered; all elements in Figs. 28A-B are not described; all the switches, capacitors and elements from SCF, selectable gain, External CAP and Voltage output in Fig. 30 are not described; elements P1 + bit1.P2, P1+bit2.P2, P1 + bit3.P2 and P1 + bit4.P2 in Fig. 31 are not described.

These rejections should be withdrawn.

First, Applicants have reviewed the cited portions of the specification and the drawings and believe that the application is clear to one of ordinary skill in the art. For example, in regard to the mixer circuit, the Examiner is directed to the specification at page 10, lines 8-10 and the mixer circuit shown in FIG. 1. This disclosure is clear to one of ordinary skill in the art. Regarding the rejection based on element 176, Applicants point out that original FIG. 5 shows element 176 as an inverter. The term "inverter" and corresponding symbol is clear to one of ordinary skill in the art. In addition, FIG. 5 has been amended, pursuant to a drawing amendment enclosed herewith under separate paper, to correct the reference designator of the inverter. This amendment brings the drawings into conformance with the specification (see page page 12, line 22). Further, the designation P1 + P2 (as it appears in FIG. 5) is clear to one of ordinary skill in the art. For example, the designation is shown in association with control of switch S13. Moreover, the specification states that switch S13 is closed on phase P1 and phase P2 (see page 14, lines 7-9, 10-11) and that switch S13 is open on phase P3 (see page 14, lines 3-7). As a further example, in regard to FIG. 6, the Examiner is directed to the specification page

7, lines 18-19, which states that "FIG. 6 illustrates one embodiment of a non-overlapping three phase clock used in the operation of the switched capacitor DAC of FIGS. 7A-7C".

Moreover, the Office Action has not provided an adequate explanation to support a rejection for lack of enablement. Such a rejection requires an **explanation** as to the factors, reasons, and evidence that lead the Examiner to conclude that the specification fails to teach how to make and use the claimed invention without **undue experimentation**. MPEP 2164.01(a) states that:

> there are **many factors** to be considered when determining whether there is sufficient evidence to support a determination that a disclosure does not satisfy the enablement requirement and whether any necessary experimentation is 'undue'. These factors include, but are not limited to:
>
> (A) The breadth of the claims;
> (B) The nature of the invention;
> (C) The state of the prior art;
> (D) The level of one of ordinary skill;
> (E) The level of predictability in the art;
> (F) The amount of direction provided by the inventor;
> (G) The existence of working examples; and
> (H) The quantity of experimentation needed to make or use the invention based on the content of the disclosure.
>
> . . .
> . . . The examiner's analysis **must consider** all the evidence related to **each of these factors** . . . .

(emphasis added)

MPEP 2164.04 states that an enablement rejection should focus on:

> those factors, reasons, and evidence that lead the examiner to conclude that the specification fails to teach how to <u>make and use</u> the **claimed invention** without <u>undue experimentation</u>, or that the scope of any enablement provided to one skilled in the art is not commensurate with the scope of protection sought by the claims . . . . For example, doubt may arise about enablement because information is missing about one or more essential parts or relationships between parts which one skilled in the art could not develop without undue experimentation. In such a case, the examiner should **specifically identify what information is missing and why** one skilled in the art could not supply the information without **undue experimentation**. See MPEP 2164.06(a). References should be supplied if possible . . . . **specific technical reasons are always required.**

(emphasis added)

Moreover, Applicants remind the Examiner of MPEP 2164.01(b), which states that "**as long as the specification discloses at least one method** for making and using the claimed invention that bears a reasonable correlation to the entire scope of the claim**, then** the enablement requirement of **35 U.S.C. 112 is satisfied**." (emphasis added).

In this instance, the Office Action has not even identified the claim limitations believed to lack enabling support, much less set forth such an explanation as to why the related disclosure is inadequate and would require undo experimentation. Applicant is left to guess what is supposedly missing from the teachings the claim require. Consequently, the rejection is improper and should be withdrawn.

If however, the Examiner continues to believe that the claims contain subject matter that is not enabled, the Examiner is requested to issue a new, non-final Office Action that provides a complete enumeration of (1) the problematic claim limitations and (2) the factual basis for any such rejection.

Paragraph 6 of the Office Action, rejects claims 5, 10, 13, 19-20, 23, 26, 33 and 36 under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As to claims 5 and 13, the Office Action states that the one to one relationship between a number of capacitor and a number of bits is vague and indefinite since it is not described and is shown in the drawings. As stated above, original claims 5, 13 recited "wherein there is a one to one relationship between a number of capacitors and a number of bits." Examples of this feature are already shown in the drawings, for example FIG. 5 (4 capacitors, 4 input bits) and FIG. 13 (4 capacitors, 4 input bits). Nonetheless, claims 5, 13 have been amended to more particular point out and distinctly claim the inventions recited by these claims.

As to claim 10, the Office Action states that it is not clear how the one or more analog signals comprises exactly one signal. Claim 10 recites "wherein the one or more analog signals comprises exactly one signal." Applicants submit that this claim is clear to one of ordinary skill in the art and that it simply limits "one or more" to "one" exactly. The rejection should be reconsidered and withdrawn.

As to claim 19, the Office Action states that there is no antecedent basis for "the same value." Applicants respectfully disagree. Claim 19 depends from claim 17, which recites "charging each of a plurality of capacitors to a value". Reconsideration is warranted.

As to claim 20, 23, 26, 33 and 36, the Office Action states that there is no antecedent basis for "the same charge." Applicants respectfully disagree. Claim 20 depends indirectly from claim 17, which recites "charging each of a plurality of capacitors ... wherein the charge on each capacitor corresponds to a weight of the value of a corresponding bit". Claim 23 depends from claim 21, which recites "charging each of a plurality of capacitors". Claim 26 depends from claim 24, which recites "charging each of a plurality of capacitors ... and connecting at least two of the plurality of capacitors to one another to share charge". Claim 33 depends from claim 31, which recites "means for charging each of a plurality of capacitors". Claim 36 depends from claim 34, which recites means for charging each of a plurality of capacitors ... and means for connecting at least two of the plurality of capacitors to one another to share charge." Thus, there is clear antecedent basis.

Claim Rejections Under 35 U.S.C. 102

In paragraph 8 of the Office Action, claims 1-65 are rejected under 35 U.S.C. 102(b) as anticipated by Da Franca et al., 5,008,674 (hereafter Da Franca).

The Office Action states that Da Franca discloses in Fig. 3, a prior art ADC comprising: a switched capacitor network receiving an equally-weighted multi-bit digital signal b0 to bw-1 and having a plurality of sub DACs each receiving an associated bit; wherein: when switches CS0, CS1, CSw-1 and S10, S11 and S1w-1 are closed, switches S00, S01 and S0w-1 are opened, all capacitors CP0, CP1 and Cpw-1 are commonly connected to reference voltage VR and having charge sharing operating state, then, subsequent to the charge sharing operating state, when switch S0 is closed, the switched capacitor network outputs at least one analog signal indicative of a sum of values of each of bit in the equally-weighted multi-bit digital signal to the common node ND which is connected to the input of a high gain inverting amplifier OA of the switched capacitor filter.

Reconsideration is requested.

Claims 1, 2-8, 40-41, 56-57

Claim 1 recites a DAC comprising "a switched capacitor network that receives a multi-bit digital signal, the switched capacitor network having a plurality of sub DACs that each receive an associated bit of the multi-bit digital signal, each of the plurality of sub DACs having an associated capacitance that receives an associated amount of charge in response to the associated

bit, wherein the associated amount of charge for each of the plurality of sub DACs is in direct proportion to a weight of the bit, the DAC having a charge sharing operating state in which **at least two of the plurality of sub DACs share charge with one another**, and having an operating state, initiated subsequent to the charge sharing operating state, in which the switched capacitor network outputs at least one analog signal indicative of a sum of values of each bit in the multi-bit signal." (emphasis added).

Da Franca does not teach or suggest a DAC that comprises a switched capacitor network having a plurality of sub DACs, where each of the plurality of sub DACs has an associated capacitance that receives an associated amount of charge, and where the DAC has an operating state in which "**at least two of the plurality of sub DACs share charge with one another**", as recited in claim 1 (emphasis added).

Da Franca discloses a digital to analog converter (Fig. 1) that uses a switched capacitor network (Fig. 3) (col. 2, lines 7-9). During clock phase 1, each capacitor CPi is charged or discharged to the voltage (0 or V_R) (col. 3, lines 20-22). During clock phase 0, the total charge on the capacitors CPi is transferred to a capacitor C_F.

However, there is no operating state in Figs. 1 or 3 in which at least two of the capacitors share charge with one another. Indeed, there is <u>no</u> operating state in which the amount of charge on any of the capacitors CPi is affected by the amount of charge on any of the other capacitors. Thus, even if Da Franca teaches a plurality of sub DACs having capacitors CPi that receive charge, as asserted in the Office Action, Da Franca does not teach or suggest a DAC with an operating state in which "**at least two of the plurality of sub DACs share charge with one another**", as recited in claim 1.

Consequently, Da Franca does not teach or suggest a DAC comprising "a switched capacitor network that receives a multi-bit digital signal, the switched capacitor network having a plurality of sub DACs that each receive an associated bit of the multi-bit digital signal, each of the plurality of sub DACs having an associated capacitance that receives an associated amount of charge in response to the associated bit, wherein the associated amount of charge for each of the plurality of sub DACs is in direct proportion to a weight of the bit, the DAC having a charge sharing operating state in which **at least two of the plurality of sub DACs share charge with one another**, and having an operating state, initiated subsequent to the charge sharing operating state, in which the switched capacitor network outputs at least one analog signal indicative of a sum of values of each bit in the multi-bit signal", as recited in claim 1 (emphasis added).

Accordingly, claim 1, and claims 2-8, 40-41, 56-57 depending therefrom, should now be allowed.

Claims 17-20, 44-45

Claim 17 recites a method of converting a multi-bit digital signal to an analog signal indicative of a sum of value of each bit in the multi-bit digital signal. The method comprises "charging each of a plurality of capacitors to a value corresponding to a value of a bit in the multi-bit signal, wherein the charge on each capacitor corresponds to a weight of the value of a corresponding bit; temporarily **connecting at least two of the plurality of capacitors to one another to share charge**; and providing at least one analog output signal indicative of a sum of values of each bit in the multi-bit signal, after disconnecting the at least two of the plurality of capacitors from one another." (emphasis added).

Da Franca does not teach or suggest a method of converting a multi-bit digital signal to an analog signal, where the method comprises charging each of a plurality of capacitors to a value corresponding to a value of a bit in the multi-bit signal; and "**connecting at least two of the plurality of capacitors to one another to share charge**", as recited in claim 17 (emphasis added).

As stated above, there is no operating state in which the amount of charge on any of the capacitors CPi is affected by the amount of charge on any of the other capacitors. Thus, Da Franca does not teach or suggest "**connecting at least two of the plurality of capacitors to one another to share charge**", as recited in claim 17 (emphasis added).

Accordingly, claim 17 and claims 18-20, 44-45 depending therefrom, should now be allowed.

Claims 27-30, 48-49

Claim 27 recites a DAC comprising "means for charging each of a plurality of capacitors to a value corresponding to a value of a bit in a multi-bit signal, wherein the charge on each capacitor corresponds to a weight of the value of a corresponding bit; **means for temporarily connecting at least two of the plurality of capacitors to one another to share charge**; and means for providing at least one analog output signal indicative of a sum of values of each bit in the multi-bit signal, after disconnecting the at least two of the plurality of capacitors from one another." (emphasis added).

As stated above with respect to claim 17, Da Franca does not teach or suggest "**connecting at least two of the plurality of capacitors to one another to share charge**" (emphasis added). Consequently, Da Franca can not (and does not) teach or suggest "**means for temporarily connecting at least two of the plurality of capacitors to one another to share charge**", as recited in claim 27 (emphasis added).

Accordingly, claim 27 and claims 28-30, 48-49 depending therefrom, should now be allowed.

Claims 37, 52-53

Claim 37 recites an integrated circuit comprising: "an integrated switched capacitor network that receives a multi-bit digital signal, the switched capacitor network having a plurality of sub DACs that each receive an associated bit of the multi-bit digital signal, each of the plurality of sub DACs having an associated capacitance that receives an associated amount of charge in response to the associated bit, wherein the associated amount of charge for each of the plurality of sub DACs is in direct proportion to a weight of the bit, the integrated switched capacitor network having a charge sharing operating state in which **at least two of the plurality of sub DACs share charge with one another**, and having an operating state, initiated subsequent to the charge sharing operating state, in which the switched capacitor network outputs at least one analog signal indicative of a sum of values of each bit in the multi-bit signal." (emphasis added).

As stated above with respect to claim 1, Da Franca does not teach or suggest a switched capacitor network having a plurality of sub DACs, where each of the plurality of sub DACs has an associated capacitance that receives an associated amount of charge, and where the DAC has an operating state in which "**at least two of the plurality of sub DACs share charge with one another**".

Consequently, Da Franca does not teach or suggest the integrated circuit of claim 37. Accordingly, claim 37, and claims 52-53 depending therefrom, should now be allowed.

Claims 58-61

Claim 58 recites a DAC comprising: "a switched capacitor network that receives a multi-bit digital signal, the switched capacitor network having a plurality of sub DACs that each receive an associated bit of the multi-bit digital signal, each of the plurality of sub DACs having

an associated capacitance that receives an associated amount of charge in response to the associated bit, wherein the associated amount of charge for each of the plurality of sub DACs is in direct proportion to a weight of the bit, the DAC having an operating state in which **at least two of the plurality of sub DACs share charge with one another**, and having an operating state in which fewer than all of the plurality of sub DACs are connected to an output terminal and the switched capacitor network outputs at least one analog signal indicative of a sum of values of each bit in the multi-bit signal." (emphasis added).

As stated above with respect to claim 1, Da Franca does not teach or suggest a DAC that comprises a switched capacitor network having a plurality of sub DACs, where each of the plurality of sub DACs has an associated capacitance that receives an associated amount of charge, and where the DAC has an operating state in which "**at least two of the plurality of sub DACs share charge with one another**".

Consequently, Da Franca does not teach or suggest the DAC of claim 58.

Accordingly, claim 58, and claims 59-61 depending therefrom, should now be allowed.

<u>Claim 62</u>

Claim 62 recites a method of converting a multi-bit digital signal to an analog signal indicative of a sum of value of each bit in the multi-bit digital signal comprising the steps of: charging each of a plurality of capacitors to a value corresponding to a value of a bit in the multi-bit signal, wherein the charge on each capacitor corresponds to a weight of the value of a corresponding bit; **connecting at least two of the plurality of capacitors to one another to share charge**; and connecting fewer than all of the plurality of sub DACs to an output terminal to provide at least one analog output signal indicative of a sum of values of each bit in the multi-bit signal." (emphasis added).

As stated above with respect to claim 17, Da Franca does not teach or suggest a method of converting a multi-bit digital signal to an analog signal, where the method comprises charging each of a plurality of capacitors to a value corresponding to a value of a bit in the multi-bit signal; and "**connecting at least two of the plurality of capacitors to one another to share charge**".

Consequently, Da Franca does not teach or suggest the method of claim 62.

Accordingly, claim 62 should now be allowed.

Claim 63

Claim 63 recites a DAC comprising: "means for charging each of a plurality of capacitors to a value corresponding to a value of a bit in a multi-bit signal, wherein the charge on each capacitor corresponds to a weight of the value of a corresponding bit; **means for connecting at least two of the plurality of capacitors to one another to share charge**; and means for connecting fewer than all of the plurality sub DACs to an output terminal to provide at least one analog output signal indicative of a sum of values of each bit in the multi-bit signal." (emphasis added)." (emphasis added).

As stated above with respect to claim 17, Da Franca does not teach or suggest "**connecting at least two of the plurality of capacitors to one another to share charge**" (emphasis added).

Consequently, Da Franca does not teach or suggest a DAC that comprises "**means for connecting at least two of the plurality of capacitors to one another to share charge**", as recited in claim 63 (emphasis added).

Accordingly, claim 63 should now be allowed.

Claim 64

Claim 64 recites an integrated circuit comprising: "an integrated switched capacitor network that receives a multi-bit digital signal, the switched capacitor network having a plurality of sub DACs that each receive an associated bit of the multi-bit digital signal, each of the plurality of sub DACs having an associated capacitance that receives an associated amount of charge in response to the associated bit, wherein the associated amount of charge for each of the plurality of sub DACs is in direct proportion to a weight of the bit, the integrated switched capacitor network having an operating state in which **at least two of the plurality of sub DACs share charge with one another**, and having an operating state in which fewer than all of the plurality of sub DACs are connected to an output terminal and the switched capacitor network outputs at least one analog signal indicative of a sum of values of each bit in the multi-bit signal." (emphasis added).

As stated above, Da Franca does not teach or suggest a switched capacitor network having a plurality of sub DACs, where each of the plurality of sub DACs has an associated capacitance that receives an associated amount of charge, and where the DAC has an operating state in which "**at least two of the plurality of sub DACs share charge with one another**".

Consequently, Da Franca does not teach or suggest the integrated circuit of claim 64. Accordingly, claim 64 should now be allowed.

Claims 12-16, 42-43, 65

As stated above with respect to claims 1 and 64, Da Franca does not teach or suggest a DAC that comprises a switched capacitor network having a plurality of sub DACs, where "**at least two of the plurality of sub DACs share charge with one another**".

Consequently, Da Franca does not teach or suggest the DAC of any of claims 12-16, 42-43 or 65 and those claims should now be allowed.

Claims 24-26, 46-47

For the same reason as given above with respect to claim 17, Da Franca does not teach or suggest the method of claim 24.

Accordingly, claim 24 and claims 25-26, 46-47 depending therefrom, should now be allowed.

Claims 34-36, 50-51

As stated above, Da Franca does not teach or suggest "**connecting at least two of the plurality of capacitors to one another to share charge**".

Accordingly, claim 34 and claims 35-36, 50-51 depending therefrom, should now be allowed.

Claims 39, 54-55

As stated above with respect to claim 1, Da Franca does not teach or suggest a switched capacitor network having a plurality of sub DACs, where "**at least two of the plurality of sub DACs share charge with one another**".

Consequently, Da Franca does not teach or suggest the integrated circuit of claim 39. Accordingly, claim 39 and claims 54-55 depending therefrom should now be allowed.

Claims 9-11

Claim 9 recites a DAC comprising "a switched capacitor network that receives an equally-weighted multi-bit digital signal and **outputs** one or more analog signals, wherein at

least one of the one or more analog signals comprises **a single packet of charge** indicative of a sum of equally-weighted values of each bit in the multi-bit signal." (emphasis added).

Da Franca does not teach or suggest "a switched capacitor network that **outputs** one or more analog signals, wherein at least one of the one or more analog signals comprises **a single packet of charge** indicative of a sum of equally-weighted values of each bit in the multi-bit signal", as recited in claim 9 (emphasis added).

Indeed, the Office Action is totally silent as to how Da Franca could possibly teach or suggest a switched capacitor network that "**outputs**" an analog signal that "comprises **a single packet of charge** indicative of a sum of equally-weighted values of each bit in the multi-bit signal", as recited in claim 9 (emphasis added).

It is true that Da Franca teaches that each of the capacitors transfers its charge to a capacitor C_F. However, this transfer of charge is in the form of several packets of charge, each of which is indicative of a particular input bit. Consequently, this transfer of charge is not a "**a single packet of charge** indicative of a sum of equally-weighted values of each bit in the multi-bit signal", as recited in claim 9.

Moreover, Da Franca does not teach or suggest "a switched capacitor network that receives an **equally-weighted multi-bit digital signal"**, as recited in claim 9 (emphasis added). Da Franca, in Fig. 3, shows a switched capacitor network that receives a multi-bit digital signal b0 to bw-1. However, Da Franca, in Fig. 3, teaches that b_0 is an LSB and that b_{w-1} is an MSB. Since bits b_0 to b_{w-1} have different weighting, the signal b0 to bw-1 is not equally weighted.

Consequently, Da Franca does not teach or suggest a DAC comprising "a switched capacitor network that receives an **equally-weighted** multi-bit digital signal and **outputs one or more analog signals, wherein at least one of the one or more analog signals comprises a single packet of charge** indicative of a sum of equally-weighted values of each bit in the multi-bit signal", as recited in claim 9 (emphasis added).

Accordingly, claim 9, and claims 10-11 depending therefrom, should now be allowed.

Claims 21-23

Claim 21 recites a method of converting a equally-weighted multi-bit digital signal to an analog signal indicative of a sum of value of each bit in the multi-bit digital signal. The method comprises "charging each of a plurality of capacitors to a value corresponding to a value of a bit in the **equally-weighted** multi-bit signal, and generating a single packet of charge on at least one

capacitor indicative of a sum of equally-weighted values of each bit in the multi-bit signal." (emphasis added).

Da Franca does not teach or suggest a method of converting a "**equally-weighted**" multi-bit digital signal to an analog signal indicative, as recited in claim 21 (emphasis added).

As stated above with respect to claim 9, Da Franca, in Fig. 3, shows a switched capacitor network that receives a multi-bit digital signal b0 to bw-1. However, Da Franca, in Fig. 3, teaches that b_0 is an LSB and that b_{w-1} is an MSB. Thus, bits b_0 to b_{w-1} have different weighting, and consequently, the signal b0 to bw-1 is not equally weighted.

Consequently, Da Franca can not teach or suggest a method of converting a **equally-weighted** multi-bit digital signal to an analog signal indicative of a sum of value of each bit in the multi-bit digital signal, where the method comprises "charging each of a plurality of capacitors to a value corresponding to a value of a bit in the **equally-weighted** multi-bit signal, and generating a single packet of charge on at least one capacitor indicative of a sum of **equally-weighted** values of each bit in the multi-bit signal." (emphasis added).

Accordingly, claim 21, and claims 22-23 depending therefrom, should now be allowed.

Claims 31-33

Da Franca, as stated above, does not teach or suggest charging each of a plurality of capacitors to a value corresponding to a value of a bit in an **equally-weighted** multi-bit signal, and generating a single packet of charge on at least one capacitor indicative of a sum of **equally-weighted** values of each bit in the multi-bit signal.

Consequently, this rejection should be withdrawn.

Claims 38

Claim 38 recites an integrated circuit comprising: "an integrated switched capacitor network that receives an **equally-weighted** multi-bit digital signal and **outputs** one or more analog signals, wherein at least one of the one or more analog signals comprises **a single packet of charge** indicative of a sum of equally-weighted values of each bit in the multi-bit signal."

As stated above with respect to claim 9, Da Franca does not teach or suggest "a switched capacitor network that **outputs** one or more analog signals, wherein at least one of the one or more analog signals comprises **a single packet of charge** indicative of a sum of equally-weighted values of each bit in the multi-bit signal".

Moreover, Da Franca does not teach or suggest "a switched capacitor network that receives an **equally-weighted multi-bit digital signal**", as recited in claim 38 (emphasis added). As stated above Da Franca, in Fig. 3, teaches that b_0 is an LSB and that b_{w-1} is an MSB. Thus, bits b_0 to b_{w-1} have different weighting, and consequently, the signal b0 to bw-1 is not equally weighted.

Consequently, Da Franca does not teach or suggest the integrated circuit of claim 38.

Accordingly, claim 38 should now be allowed.

Provisional Double Patenting Rejections

Paragraph 10 of the Office Action states that claims 1-65 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting over claims 1-9 and 30 of co-pending Application No. 09/575,560. The Office Action states that although the conflicting claims are not identical, they are not patentably distinct from each other.

Applicants note that these rejections are provisional and therefore do not require a response at this time. However, Applicants expressly reserve the right to respond at a future time.

Conclusion

This application should now be in condition for allowance. A notice to this effect is respectfully requested. If the Examiner believes, after this Amendment, that the application is not in condition for allowance, the Examiner is requested to call the Applicants' Attorney at the number listed below.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicants hereby request any necessary extension of time. If there is a fee occasioned by this response, including any extension fee that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,

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MARKED-UP SPECIFICATION

Please replace the paragraph beginning on line 28, page 9, with the following:

FIG. 1 is a block diagram of one embodiment of a portion of a handset 50 for a mobile communication system. The handset 50 includes an input portion having a transducer 54 that receives an input signal 56, e.g., a voice or other acoustical signal, representing information to be communicated via the mobile communication system. The transducer 54 converts the input signal 56 into an electrical signal, typically an analog signal, which is supplied to an analog-to-digital converter (ADC) 58, for example a voiceband ADC. The ADC 58 periodically samples the electrical signal and generates a sequence of multi-bit digital signals, which are supplied to a digital baseband processor 60. The baseband processor 60 performs further signal processing, including for example, compression. The output of the baseband processor 60 is supplied to burst store stage 62, which feeds a GMSK modulator 64. The GMSK modulator 64 produces multi-bit digital signals, which is supplied via signal lines, represented by a signal line 66, to a digital to analog conversion system 68. The digital to analog conversion system 68 converts the sequence of multi-bit digital signals into an analog signal, which is supplied via signal line 70 to an output portion 72. The output portion 72 includes a mixer [72] 74 that receives the analog signal on signal line 70 and feeds a transmitter 76, which in turn transmits the signal. DAC can be used in any digital to analog conversion.

Please replace the paragraph beginning on line 21, page 20, with the following:

FIG. 15 is a block diagram of another embodiment of the SC DAC 150, which is similar to the SC DAC 150 illustrated in FIGS. [9, 10A-10C] 13, 14A-14C, except that the SC DAC 150 of FIG. 15 further comprises a switch [148] S48, a switch [149] S49, and a switch [150] S50. A first terminal of the switch S48 is connected to the second terminal of the charge sharing switch S43. A first terminal of the switch S49 is connected to the second terminal of the charge sharing switch S45. A first terminal of the switch S50 is connected to the second terminal of the charge sharing switch S46. Each of the switches S48, S49, and S50 may, but need not serve one or more of the functions noted hereinbelow. In one embodiment, one purpose of the switches S48, S49, S50 is to provide parasitic capacitance similar to that of output switch S47, so as to help cancel the effect of the parasitic capacitance of switch S47.

MARKED-UP CLAIMS

5. (Amended) The DAC of claim 1, wherein [there is a one to one relationship between a number of capacitors and a number of bits] for each of the plurality of sub DACs, the associated capacitance comprises a single capacitor.

13. (Amended) The DAC of claim 12, wherein [there is a one to one relationship between a number of capacitors and a number of bits] for each of the plurality of sub DACs, the associated capacitance comprises a single capacitor.

37. (Twice Amended) An integrated circuit comprising:

an integrated switched capacitor network that receives a multi-bit digital signal, the switched capacitor network having a plurality of sub DACs that each receive an associated bit of the multi-bit digital signal, each of the plurality of sub DACs having an associated capacitance that receives an associated amount of charge in response to the associated bit, wherein the associated amount of charge for each of the plurality of sub DACs is in direct proportion to a weight of the bit, the [DAC] integrated switched capacitor network having a charge sharing operating state in which at least two of the plurality of sub DACs share charge with one another, and having an operating state, initiated subsequent to the charge sharing operating state, in which the switched capacitor network outputs at least one analog signal indicative of a sum of values of each bit in the multi-bit signal.

64. (Amended) An integrated circuit comprising:

an integrated switched capacitor network that receives a multi-bit digital signal, the switched capacitor network having a plurality of sub DACs that each receive an associated bit of the multi-bit digital signal, each of the plurality of sub DACs having an associated capacitance that receives an associated amount of charge in response to the associated bit, wherein the associated amount of charge for each of the plurality of sub DACs is in direct proportion to a weight of the bit, the [DAC] integrated switched capacitor network having an operating state in which at least two of the plurality of sub DACs share charge with one another, and having an operating state in which fewer than all of the plurality of sub DACs are connected to an output

terminal and the switched capacitor network outputs at least one analog signal indicative of a sum of values of each bit in the multi-bit signal.